Remarks

Applicant respectfully requests reconsideration of this application as amended. Claims 13, 15, 20, 22, 26, and 28 have been amended. Claims 14, 21, and 27 have been canceled. No claims have been added. Therefore, claims 13, 15-20, 22-26, and 28-31 are presented for examination.

35 U.S.C. §103(a) Rejection

Claims 13-31 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tsuyoshi et al. (U.S. Patent No. 4,949,325) in view of Huber (U.S. Patent No. 4,110,557) further in view of Inada et al. (U.S. Patent No. 5,534,807). Applicant submits that the present claims are patentable over Tsuyoshi in view of Huber and Inada.

Briefly, Tsuyoshi discloses a method of recording/reproducing information associated with an apparatus and recording medium. Huber discloses a phase lock oscillator system employing a phase and frequency detector which receives data pulses and a clocking signal modulated to include only the clocking pulses for generating an error signal to regulate the voltage controller oscillator. Inada discloses a sampling circuit that is not susceptible to an influence of structural components and environmental changes.

Claim 13, as amended, recites:

> A method for recovering a digital data signal (D_{out}) and a clock signal (Ck_{out}) comprising:
> receiving a data signal (D_{in}) including a plurality of successive bits;
> generating, from the data signal (D_{in}), the clock signal (Ck_{out}) with a resonator circuit;
> delaying the data signal (D_{in}) to compensate for a delay created by the generating the clock signal (Ck_{out}) so that the data signal(D_{in}) is synchronized with the clock signal (Ck_{out});
> phase locking the clock signal (Ck_{out}) to the delayed data signal by:

measuring, via a phase detector, a phase difference between the clock signal (Ck_{out}) and the delayed data signal wherein measuring the phase difference includes sampling in the phase detector the delayed data signal with the clock signal (Ck_{out}) in three flip-flops at three different points in time; and

time delaying the clock signal (Ck_{out}) based on the phase difference by generating a first steering signal based on the phase difference and controlling, with the first steering signal, a controlled delay unit;

sampling the delayed data signal at approximately the center of each bit with the delayed clock signal (Ck_{out}); and

generating, as a result of the sampling, the digital data signal (D_{out}).

Applicant submits that Tsuyoshi does not disclose or suggest phase locking a clock signal to a delayed data signal by...time delaying the clock signal (Ck_{out}) based on the phase difference by generating a first steering signal based on the phase difference and controlling, with the first steering signal, a controlled delay unit, as recited by claim 13. Applicant can find no disclosure or suggest of such a feature anywhere in Tsuyoshi. Therefore, Tsuyoshi does not disclose or suggest the cited features of claim 13.

Applicant further submits that Huber does not disclose or suggest phase locking a clock signal to a delayed data signal by...time delaying the clock signal (Ck_{out}) based on the phase difference by generating a first steering signal based on the phase difference and controlling, with the first steering signal, a controlled delay unit. The Office Action does not rely on Huber to disclosure this feature nor can applicant can any disclosure or suggestion of such a feature in Huber. Therefore, Huber does not disclose or suggest the cited features of claim 13.

Applicant additionally submits that Inada does not disclose or suggest phase locking a clock signal to a delayed data signal by...time delaying the clock signal (Ck_{out}) based on the phase difference by generating a first steering signal based on the phase difference and controlling, with the first steering signal, a controlled delay unit. The Office Action does not

rely on Inada to disclosure this feature nor can applicant can any disclosure or suggestion of such a feature in Huber.. Therefore, Inada does not disclose or suggest the cited features of claim 13.

As none of Tsuyoshi,Huber, or Inada individually disclose phase locking a clock signal to a delayed data signal by...time delaying the clock signal (Ck_{out}) based on the phase difference by generating a first steering signal based on the phase difference and controlling, with the first steering signal, a controlled delay unit, any combination of Tsuyoshi, Huber, and Inada also does not disclose or suggest such a feature. Therefore, claim 13, as well as its dependent claims, it patentable over Tsuyoshi and Huber in view of Inada.

Independent claims 20 and 26 also recite, in part, phase locking a clock signal to a delayed data signal by...time delaying the clock signal (Ck_{out}) based on the phase difference by generating a first steering signal based on the phase difference and controlling, with the first steering signal, a controlled delay unit. As discussed above, Tsuyoshi and Huber in view of Inada does not disclose or suggest such a feature. Therefore, claims 20 and 26 are patentable over Tsuyoshi and Huber in view of Inada for the reasons discussed above with respect to claim 13.

Applicant respectfully submits that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Ashley R. Ott
Reg. No. 55,515

12400 Wilshire Boulevard
7th Floor
Los Angeles, California 90025-1026
(303) 740-1980